

Exciter ST6C

IEEE Std 421.5-2016 Exciter with static potential and compound source with field current limiter

States:

- 1 – V_M
- 2 – Sensed V_T
- 3 – V_A
- 4 – V_G

The diagram illustrates the control logic for the Exciter ST6C. It starts with a reference voltage V_{REF} and a sensed terminal voltage V_T (State 2). The sensed V_T is compared with upper (V_{UEL}) and lower (V_{LEL}) limits (State 1) at a summing junction. The resulting signal passes through an HV gate and an LV gate. The output of the LV gate is compared with V_{UEL} and V_{LEL} limits (State 3) at another summing junction. The signal then passes through a K_{PA} block and a K_{IA} block. The output is compared with V_{Amin} and V_{Amax} limits at a third summing junction. The signal then passes through a K_{FF} block and a K_M block. The output is compared with V_{Rmin} and V_{Rmax} limits at a fourth summing junction. The signal then passes through an HV gate and an LV gate. The output of the LV gate is compared with V_{SCLuel} and V_{SCLoel} limits (State 4) at a fifth summing junction. The signal then passes through a K_G block and a 1/(1+sT_G) block. The output is compared with V_{Mmin} and V_{Mmax} limits (State 1) at a sixth summing junction. The signal then passes through a 1/(1+sT_A) block. The output is compared with V_{Bmin} and V_{Bmax} limits at a seventh summing junction. The signal then passes through a K_{CI} block and a K_{LR} block. The output is compared with I_{LR} limits at an eighth summing junction. The signal then passes through a K_N block and a K_{FD} block. The output is compared with I_{Nmin} and I_{Nmax} limits at a ninth summing junction. The final output is the field current I_N , which is used to calculate the field flux $F_{EX} = f(I_N)$ and the terminal voltage V_T .

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Exciter ST6C Footnotes:

